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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,637	01/20/2004	Chantal Auricchio	854063.737	8266

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EXAMINER

TRAN, ANH Q

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

OK

Office Action Summary	Application No. 10/760,637	Applicant(s) AURICCHIO ET AL.	
	Examiner Anh Q. Tran	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-14 is/are allowed.
- 6) ☒ Claim(s) 1-3, 8 and 9 is/are rejected.
- 7) ☒ Claim(s) 4-7, 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 8, 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Pass et al. (5,949,710).

Claim 1, Pass shows a nonvolatile switch, comprising:

an input terminal (GV1);

an output terminal (GH1);

a selection terminal (CG);

a first (DL) and a second (SL) biasing terminal;

a memory element (1516, col. 25, lines 35-37) of flash type, having a first conduction region (drain) connected to said first biasing terminal and a second conduction region (source) connected to said second biasing terminal;

a pass transistor (1525), having a first conduction region (drain) connected to said input terminal and a second conduction region connected to said output terminal (source); and

a pair of common-gate regions, having a common floating gate region (1520) and a common control gate region (CG), which are capacitively coupled together, said memory element and said pass transistor sharing said common-gate regions and

integrated adjacent to each other (col. 25, lines 37-41), and said common control-gate region being connected to said selection terminal,

wherein the switch is a programmable switch that can pass or block data from the input terminal to the output terminal based on programmable ON/OFF operation of the switch (conduct or nonconduct, col. 10, lines 2-6 and col. 25, lines 42-61).

Claim 2, Pass shows the switch according to claim 1, further comprising a second pass transistor (1530), having a first conduction region connected to an own input terminal (GH2) and a second conduction region connected an own output terminal (GV2), said second pass transistor, said memory element and said pass transistor sharing said common-gate regions (CG and 1520).

Claim 3, Pass shows switch according to claim 1 wherein said common gate regions extend parallel to one another on top of said body of semiconductor material (1730, Fig. 17).

The limitations of claim 8 is rejected as above claim 1.

The apparatus described above is applicable to the method claim 9.

Allowable Subject Matter

3. Claims 4-7, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
4. The following is a statement of reasons for the indication of allowable subject matter:

-wherein said body accommodates a first and a second active area separated by an insulating region, said common-gate regions extending in a direction transverse to, and on top of, said first and second active areas, said first active area forming said first and second conduction regions of said memory element, and said second active area forming said first and second conduction regions of said pass transistor.

- wherein said program biasing comprises:
- applying a first and a second potential, respectively, to a first and a second conduction region of said memory element, and applying a third potential to said common control gate region of said memory element and of said pass transistor in a writing step; leaving said first conduction region of said memory element floating, applying a fourth potential to said second conduction region of said memory element, and applying a fifth potential to said common control gate region of said memory element and of said pass transistor in an erasing step; and leaving said first conduction region of said memory element floating, applying a reference potential to said second conduction region of said memory element, applying a sixth potential to said common control gate region of said memory element and said pass transistor, and detecting possible data on an output terminal of said pass transistor.

5. Claims 11-14 are allowed.

6. The following is an examiner's statement of reasons for allowance: with respect to claim 11, in addition to other limitations in the claim, the prior art of record fails to teach, disclose or render obvious the applicant's invention as claimed, particularly the

feature describing a body of semiconductor material wherein said common gate regions extend another on top of said body of semiconductor material, wherein said body parallel to one accommodates a first and a second active area separated by an insulating region, said common- gate regions extending in a direction transverse to, and on top of said first and second active areas, said first active area forming said first and second conduction regions of said memory element, and said second active area forming said first and second conduction regions of said pass transistor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Lipp et al (5,764,096) discloses a non-volatile reprogrammable switch and a memory structure which share floating gate and control gate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



12/1/05